Amendments to the Specification:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to the following co-pending U.S. Patent Applications that are each incorporated by reference as if set forth in full in this application:

"INPUT PIPELINE REGISTERS FOR A NODE IN AN ADAPTIVE COMPUTING ENGINE," Serial No. 10/626,479 ~~[TBD]~~, filed 7/23/2003 ~~[TBD]~~ (Our Ref. No. 021202-003720US);

"CACHE FOR INSTRUCTION SET ARCHITECTURE USING INDEXES TO ACHIEVE COMPRESSION," Serial No. 11/628,083 ~~[TBD]~~, filed 7/24/2003 ~~[TBD]~~ (Our Ref. No. 021202-003730US);

"METHOD FOR ORDERING OPERATIONS FOR SCHEDULING BY A MODULO SCHEDULER FOR PROCESSORS WITH A LARGE NUMBER OF FUNCTION UNITS AND RECONFIGURABLE DATA PATHS," Serial No. 10/146,857, filed on May 15, 2002 (Our Ref. No. 021202-002700US);

"UNIFORM INTERFACE FOR A FUNCTIONAL NODE IN AN ADAPTIVE COMPUTING ENGINE," Serial No. 10/443,554 ~~[TBD]~~, filed on May 21, 2003 (Our Ref. No. 021202-003400US);

"HARDWARE TASK MANAGER FOR ADAPTIVE COMPUTING," Serial No. 10/443,501 ~~[TBD]~~, filed on May 21, 2003 (Our Ref. No. 021202-003500US);

"ADAPTIVE INTEGRATED CIRCUITRY WITH HETEROGENEOUS AND RECONFIGURABLE MATRICES OF DIVERSE AND ADAPTIVE COMPUTATIONAL UNITS HAVING FIXED, APPLICATION SPECIFIC COMPUTATIONAL ELEMENTS," Serial No. 09/815,122, filed on March 22, 2001;